REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 35-38 have been amended and claim 27 has been canceled. No new matter has been added. Claims 1-26 and 28-43 remain pending.

Objections to the Drawings

The drawings have been objected to because, in Figure 11, "DBUS" is depicted with a left-hand arrow instead of a right-hand arrow. Applicant has amended Figure 11 to address the reason for objection. An Annotated Marked-Up Drawing Sheet showing the proposed change in red ink is enclosed herewith, together with a Replacement Drawing Sheet incorporating the proposed change. No new matter has been added.

Objections to the Specification

The specification has been objected due to certain informalities. Applicant has amended the specification to correct the informalities and to correct a minor typographical error. No new matter has been added.

Claim Rejections -- 35 U.S.C. § 112

Claims 36 and 38 have been rejected under 35 U.S.C. § 112 as being incomplete for omitting essential structural cooperative relationships of elements and as lacking antecedent basis for certain expressions therein. Applicant has amended claims 35-38 to address the section 112 rejection and respectfully requests that the rejection is overcome. No new matter has been added.

Claim Rejections -- 35 U.S.C. § 102

Claims 1-18 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,597,595 to Ichiriu et al. ("Ichiriu").

Claims 1-22, 25-36 and 39-43 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,539,324 to Miyatake et al. ("Miyatake").

Claim 27 has been canceled without acquiescence to the reason for rejection, rendering the rejection of that claim moot.

Applicant has enclosed a Declaration of Prior Invention pursuant to 37 CFR § 1.131 to establish invention of the subject matter recited in claims 1-26 and 28-43 prior to the June 19, 2001 effective date of Miyatake, and therefore prior to the August 3, 2001 effective date of

Ichiriu. Applicant respectfully requests that the section 102 rejections be withdrawn in view of the Declaration of Prior Invention.

Claim Rejections -- 35 U.S.C. § 103(a)

Claims 24, 37 and 38 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Ichiriu and have also been rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyatake in view of Ichiriu.

Claim 23 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyatake in view of U.S. Patent No. 6,341,092 to Agrawal.

Applicant respectfully requests that these rejections be withdrawn in view of the Declaration of Prior Invention.

Conclusion

Applicant respectfully submits that claims 1-26 and 28-43 are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

Authorization is hereby given to charge deposit account 501914 for any fee deficiency associated with this Amendment.

Respectfully submitted,

SHEMWELL GREGORY & COURTNEY LLP

Date October 22, 2004

Charles E. Shemwell, Reg. No. 40,171
Tel. 408-236-6645

EXHIBIT A

Application No. 10/004,209

Atty. Docket No. NLMLP143 (formerly NLM.P005) *PATENT*

IN THE UNITED STATES PATENT OFFICE

In Re Patent Application of:

Huse, Charles C.

Application No.: 10/004,209

Filed: November 1, 2001

For: METHOD AND APPARATUS FOR TESTING A CONTENT ADDRESSABLE MEMORY DEVICE

Examiner: Trimmings, John P.

Art Unit: 2133

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Declaration of Charles C. Huse to Establish Prior Invention Under 37 C.F.R. § 1.131

I, Charles C. Huse, hereby declare:

1. I am the sole inventor named in the above-referenced patent application (hereinafter, the "Application").

2. I conceived the invention claimed in the Application in the United States while working as an employee of NetLogic Microsystems, Inc. of Mountain View, California.

3. I conceived the invention claimed in the Application at least prior to June 19, 2001, the effective date of a reference relied upon to reject claims of the Application (the "Effective Date"), as demonstrated by facts set forth in Exhibit A enclosed herewith.

4. I am informed and believe that reasonable diligence in constructively reducing the invention to practice was exercised from just prior to the Effective Date to the November 1, 2001 filing date of the Application as demonstrated by the enclosed Declarations of Lawrence M. Cho, the patent attorney that prepared the Application, and Roland B. Cortes, the in-house patent counsel of NetLogic Microsystems, Inc.

5. Exhibit A consists of four whiteboard printouts prepared by me prior to the Effective Date during an invention disclosure meeting between me and Mssrs. Cho and Cortes. An accurate reproduction of legible material in each of the whiteboard printouts is included in Exhibit A to aid examination.

6. A CAM device having a CAM array, priority encoder, counter and compare logic coupled and/or operable in the manner recited in claims 1, 2, 11, 12, 16, 18, 19, 29-32, and 39-43 is disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be present in the CAM device disclosed in Exhibit A, in view of, for example, the CAM array, priority encoder (PE), counter (ACTR) and compare logic (Compare) disclosed in Exhibit A, page 4 (Exhibit A4).

7. Address logic as recited in claims 3, 4, 13, 15, and 21 and write circuitry as recited in claim 10 is disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be

present in the CAM device disclosed in Exhibit A, in view of, for example, the arrow extending from ACTR to the CAM array in Exhibit A4 and by the reference in Exhibit A4 to "writ[ing] unique data to each entry, using ACTR."

8. A multiplexer as recited in claims 5, 6 and 9 is disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be present in the CAM device disclosed in Exhibit A, in view of, for example, the multiple address sources used to access the CAM array including, without limitation, ACTR as disclosed in Exhibit A4 and highest priority match index as disclosed in Exhibits A2 and A3 by the reference "set empty@hpm."

9. An instruction decoder as recited in claims 7, 14, 17, 22 and 28 is disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be present in the CAM device disclosed in Exhibit A, in view of, for example, the instruction decoder ("INSTR") and instruction bus ("IBUS") disclosed in Exhibit A3.

10. A multiplexer as recited in claim 8 is disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be present in the CAM device disclosed in Exhibit A, in view of, for example, the multiple sources of comparand data including, without limitation, ACTR as disclosed in Exhibit A4 (dashed line extending from ACTR to Comparand and reference to "copy[ing] ACTR to comparand & compare") and data as disclosed in Exhibit A3 ("write comparand = (data)").

11. A comparand register as recited in claim 10 is disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be present in the CAM device disclosed in Exhibit A, in view of, for example, the comparand register ("Comparand") disclosed in Exhibit A4.

12. A CAM array having a plurality of rows of CAM cells coupled to a counter to receive a counter value for storage in at least one of the rows of the CAM cells as recited in claim 15 is disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be present in the CAM device disclosed in Exhibit A, in view of, for example, the references in Exhibit A4 to "writ[ing] unique data to each entry, using ACTR (write data n to row n)" and a loop that includes "writ[ing] ACTR to memory@ACTR, incr."

13. A test system comprising a tester that generates test signals and a CAM device coupled to receive the test signals as recited in claim 19; compare logic having an output coupled to the tester as recited in claim 20; wherein the test signals include instructions for the CAM device as recited in claim 22; wherein the tester comprises automated test equipment (ATE) as recited in claim 23; and wherein the tester comprises a processor as recited in claim 24 are disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be present in the test system disclosed in Exhibit A, in view of, for example, the reference to "logic tester" in Exhibit A1, the reference to "vector length" in Exhibit A2, the reference to "compare[ing] index to ACTR," "if match, assert a flag," and "in vector file, monitor this flag" in Exhibit A2, and the reference to "monitor[ing] (ACTR vs. index) flag" in a loop in Exhibit A4.

14. A test system comprising a tester, counter, compare logic, and CAM device as recited in claim 25; compare logic having an output coupled to the tester as recited in claim 26; and wherein the test signals include instructions for the CAM device as recited in claim 28 are disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be present in the test system disclosed in Exhibit A, in view of, for example, the CAM array, priority encoder (PE), counter (ACTR) and compare logic (Compare) disclosed in Exhibit A4, the reference to "logic tester" in Exhibit A1, the reference to "vector length" in Exhibit A2, the reference to "compare[ing] index to ACTR," "if match, assert a flag," and "in vector file, monitor this flag" in Exhibit A2, and the

reference to "monitor[ing] (ACTR vs. index) flag" in a loop in Exhibit A4.

15. A method of operating a CAM device wherein the data stored in a plurality of rows of CAM cells is the same for each of the rows of CAM cells as recited in claim 33; masking CAM cells in a first row of CAM cells corresponding to a first counter value and identifying whether an index matches the first counter value as recited in claim 34; unmasking the first row of CAM cells and incrementing a counter to a second counter value as recited in claim 35; and masking the CAM cells in a second row of the CAM cells corresponding to the second counter value, repeating the steps of claim 32 and identifying whether the index matches the second counter value as recited in claim 36 are disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be part of a method of operating the CAM device disclosed in Exhibit A, in view of, for example, the "Example" set forth in Exhibit A1 in which memory is filled with a local mask value of 0000 and a data value of 0000 (fill memory: "local mask = 0000," "data = 0000"), ACTR is initialized to a first counter value ("ACTR – 0"), the local mask is set to FFFF in the row pointed at by ACTR thus masking the entry at row 0 ("wlm = FFFF"), a compare operation is performed to identify whether the index matches the first counter value ("compare => match" and "index = row#"), a 0 is walked across the local mask ("wlm = 7FFF," "wlm = BFFF," ...) before the local mask is cleared in the row pointed at by ACTR ("wlm – 0000"), ACTR is incremented to a second count value ("Increment ACTR"), and the operations of masking comparing are repeated.

16. A method of operating a CAM device wherein the data stored in a plurality of rows of CAM cells is the same for each of the rows of CAM cells as recited in claim 33; identifying whether an index matches a first counter value, invalidating the row of CAM cells that corresponds to the index, and incrementing a counter to a second counter value as recited in claim 37; and repeating the steps of claim 32, identifying whether the index matches the second counter value, and invalidating the row of CAM cells that corresponds to the index as recited in claim 38 are disclosed in Exhibit A, or would have been understood by one of ordinary skill in the art to be part of a method of operating the CAM device disclosed in Exhibit A, in view of, for example, "Example 2" set forth in Exhibit A2 in which memory is filled with a local mask value of 0000 ("wlm – 0000") and the same data value in each row ("write memory = (data)"), the data value stored in memory is written to the comparand ("write comparand = (data)"), the comparand is compared with contents of the CAM array to generate an index ("compare => match :index = 0"), the index is compared to ACTR to identify whether the index matches the counter value maintained within ACTR ("increment ACTR to match expected index," and "compare index to ACTR"), invalidating the row of CAM cells that corresponds to the index ("set empty@hpm"), and repeating the steps of comparing the comparand with content of the CAM array to generate an index, identifying whether the index matches the counter value maintained within ACTR, and invalidating the row of CAM cells that corresponds to the index.

I hereby declare that all statements herein made of my own knowledge are true and all statements made on information and belief are believed to be true. I hereby acknowledge that willful false statements and the like are punishable by fine or imprisonment, or both (18 US.C. § 1001) and may jeopardize the validity of the Application or any patent issuing thereon.

Respectfully submitted,

Date 10/22/04 Charles C. Huse

Charles C. Huse

Atty. Docket No. NLMI.P143 (formerly NLM.P005) *PATENT*

IN THE UNITED STATES PATENT OFFICE

In Re Patent Application of:

Huse, Charles C.

Application No.: 10/004,209

Filed: November 1, 2001

For: METHOD AND APPARATUS FOR TESTING A CONTENT ADDRESSABLE MEMORY DEVICE

Examiner: Trimmings, John P.

Art Unit: 2133

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Declaration of Lawrence M. Cho

I, Lawrence M. Cho, hereby declare:

1. I am a registered patent attorney (Registration No. 39,942) and was engaged by NetLogic Microsystems, Inc. to prepare the above-identified patent application (hereinafter, the "Application").
2. The invention claimed in the Application was disclosed to me by Charles C. Huse at least prior to June 19, 2001, the effective date of a reference relied upon to reject claims of the Application (the "Effective Date").
3. I completed a reasonable backlog of other cases from a time just prior to the Effective date to July 11, 2001.
4. I rendered services related to preparation of the Application regularly from July 12, 2001 to August 19, 2001 culminating in a draft of the Application sent to Roland B. Cortes, the in-house patent counsel of NetLogic Microsystems, Inc., on or about August 21, 2001.
5. I received instruction from Mr. Cortes on or about October 31, 2001 to file the Application and did file the Application on November 1, 2001.

I hereby declare that all statements herein made of my own knowledge are true and all statements made on information and belief are believed to be true. I hereby acknowledge that willful false statements and the like are punishable by fine or imprisonment, or both (18 US.C. § 1001) and may jeopardize the validity of the Application or any patent issuing thereon.

Respectfully submitted,

Date 10/22/2004

L M. Cho

Lawrence M. Cho

Atty Docket No. NLMI.P143 (formerly NLM.P005) *PATENT*

IN THE UNITED STATES PATENT OFFICE

In Re Patent Application of:

Huse, Charles C.

Application No.: 10/004,209

Filed: November 1, 2001

For: METHOD AND APPARATUS FOR TESTING A CONTENT ADDRESSABLE MEMORY DEVICE

Examiner: Trimmings, John P.

Art Unit: 2133

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Declaration of Roland B. Cortes

I, Roland B. Cortes, hereby declare:

1. I am a patent attorney (Registration No. 39,152) and have been continuously employed by NetLogic Microsystems, Inc. to manage patent-related matters, among other things, at least since 1999.
2. Exhibit A, enclosed herewith, consists of four whiteboard printouts that were prepared by Charles C. Huse prior to the Effective Date during an invention disclosure meeting relating to the above-identified patent application (hereinafter, the "Application") attended by me, Mr. Huse and Lawrence M. Cho, the patent attorney that prepared the Application.
3. I received a draft of the Application on or about August 21, 2001 from Mr. Cho.
4. I provided the draft Application to Mr. Huse with instruction to review and provide comments back to me. I forwarded comments provided by Mr. Huse, if any, to Mr. Cho.
5. It was my standard practice, at least during the period from August 21, 2001 to the November 1, 2001 filing date of the Application, to personally review all or substantially all draft patent applications prior to their filing.
6. During the period from August 21, 2001 to November 1, 2001, I diligently reviewed at least ten (10) draft patent applications in turn, including the draft Application, and instructed outside patent counsel regarding changes required in each.
7. I instructed Mr. Cho to file the Application on or about October 31, 2001.

I hereby declare that all statements herein made of my own knowledge are true and all statements made on information and belief are believed to be true. I hereby acknowledge that willful false statements and the like are punishable by fine or imprisonment, or both (18 US.C. § 1001) and may jeopardize the validity of the Application or any patent issuing thereon.

Respectfully submitted,

Date October 22, 2004

Roland B. Cortes, Senior Director of Legal Affairs
NetLogic Microsystems, Inc.

Example:

fill memory: local word = 0000

data = 0000

write compared = FFFF

ACTR = 0

wdm = FFFF...

compare → match

wdm = 7FFF...

compare → mismatch

wdm = BFFF...

compare → mismatch

} walk 0 across, local word

wdm = 0000...

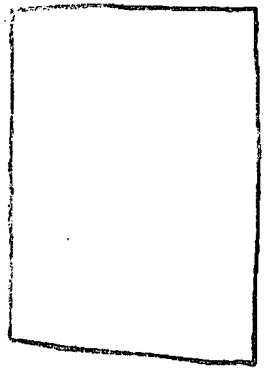
Increment ACTR ← index = row #

: I can't check this currently.

because logic tester doesn't allow a variable in the vector

Example 2:

fill the memory:
wlm = 0000
write memory (data)



write compared = (data)
(compare = match : index=0
set empty@hpm
Compare = match : index = 1

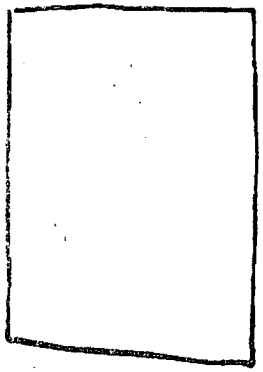
write length = 2x(table depth) + 1

if I could increment the expected index:
write comp.
loop (table depth):
compare
set empty@hpm

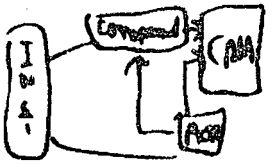
My ideas: - increment ACTR to match expected index
- compare index to ACTR
if match, assert a flag
- in vector file, monitor this flag

Example:

fill the memory:
write mem = 0000
write memory = (data)
← already a loop



write compound = (data)
(compare = match : index=0
set empty @hpm
compare = match : index=1
⋮



write length = 2x(table depth) + 1

if I could increment the expected index:
write comp.
loop (table depth):
compare
MOP ← clear regs
set empty @hpm ← data mem
increment AETR ← my idea requires this

INDEX	RAM
0000 00...	LLL HH...

Ex:

- write unique data to each entry, using ACTR (write data n to row n)
- write data 0 (data in row 0) to compand & compare
  ⇒ match, index = 0
  ⋮
- write data n to compand & compare
  ⇒ match, index = n

Modify to loop

- write ACTR to memory @ ACTR, inc.
- loop:
  - copy ACTR to compand & compare
    ⇒ match, monitor (ACTR vs. index) flag
  - increment ACTR

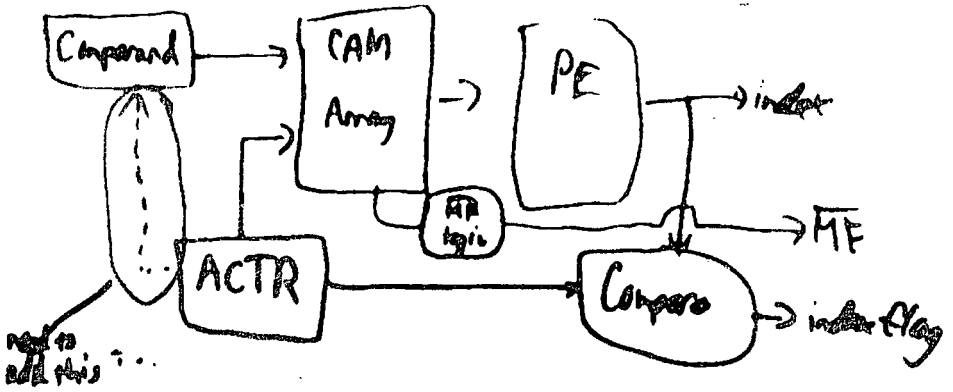
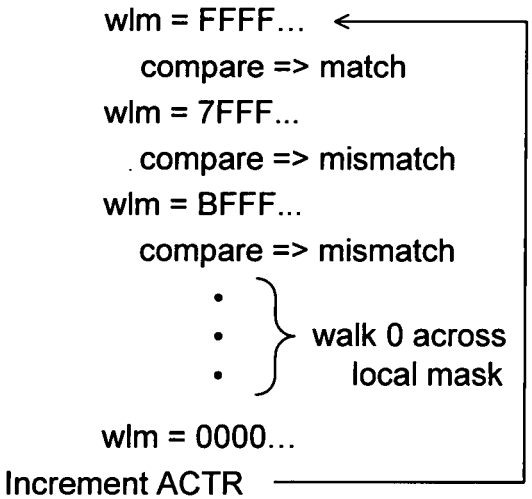


Exhibit A1
(Reproduction)

Example:

fill memory: local mask = 0000
data = 0000

write comparand = FFFF
ACTR = 0

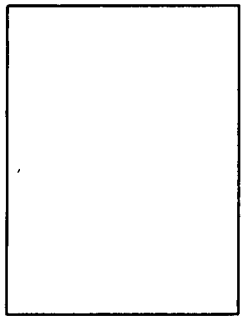


← index = row#

:I can't check this currently
because logic tester doesn't allow a variable
in the vector

Exhibit A2
(Reproduction)

Example 2:



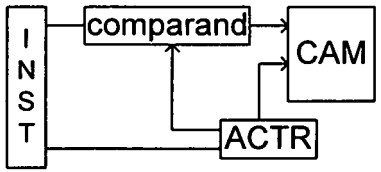
fill the memory
wlm = 0000
write memory = (data)
write comparand = (data)
compare => match : index = 0
set empty@hpm
compare => match : index = 1
•
•
•

vector length = 2 x (table depth) + 1

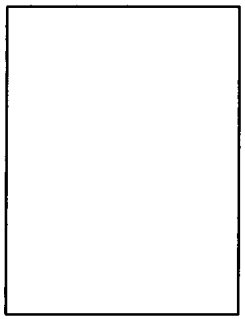
if I could increment the expected index:
write comp.
loop (table depth):
compare
set empty@hpm

My idea: - increment ACTR to match expected index
- compare index to ACTR
if match, assert a flag
- in vector file, monitor this flag

Exhibit A3
(Reproduction)



Example 2:



fill the memory
wlm = 0000
write memory = (data)
write comparand = (data)
compare => match : index = 0
set empty@hpm
compare => match : index = 1
•
•
•

← already a loop

vector length = 2 x (table depth) + 1

if I could increment the expected index:
write comp.
loop (table depth):
compare
NOP ← check flags
set empty@hpm ← check [redacted]
increment ACTR <= my idea requires this

IBUS	RBUS
0010 00...	LLL HH...

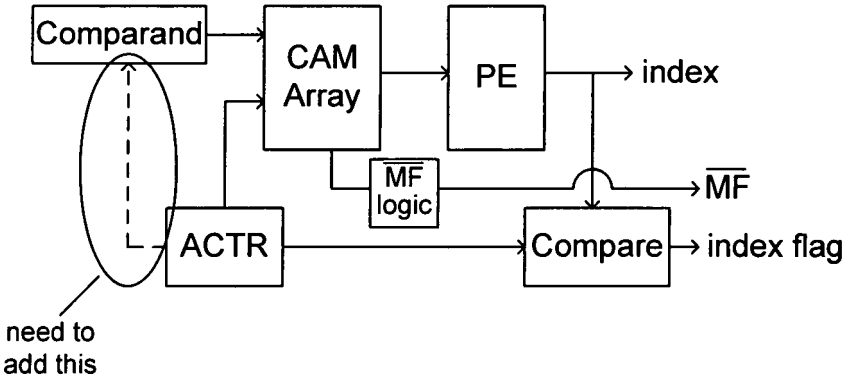
Exhibit A4
(Reproduction)

Ex:

- write unique data to each entry, using ACTR (write data n to row n)
- write data 0 to comparand & compare (data in row 0)
  => match, index = 0
  •
  •
  •
- write data n to comparand & compare
  => match, index = n

Modify to loop

loop
- wlm = 0000
- write ACTR to memory@ACTR, incr.
- copy ACTR to comparand & compare
  => match, monitor (ACTR vs. index) flag
- increment ACTR



Annotated, Marked-UP Drawing (Sheet 1 of 1)

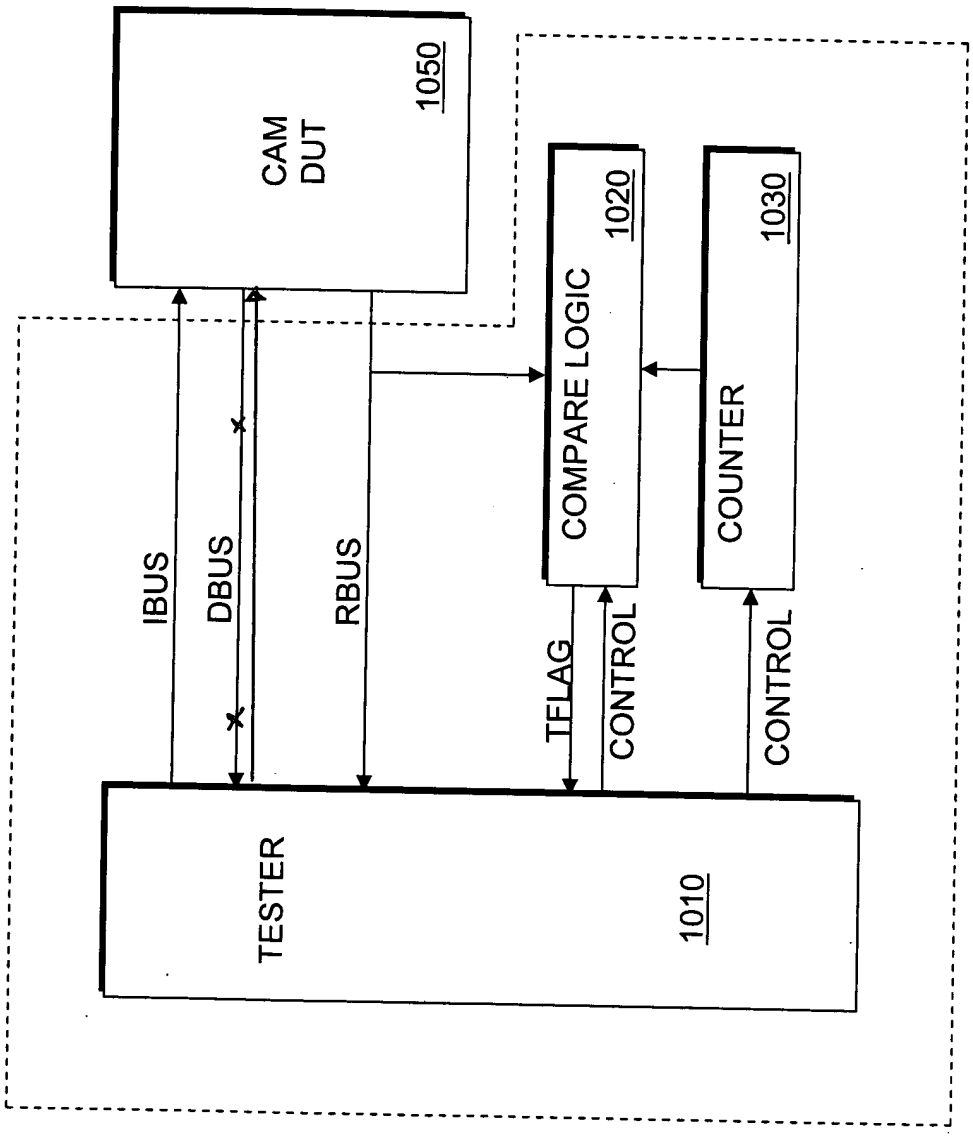


FIG. 11